



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/784,705

02/23/2004

Chung-Hui Chen

N1280-00100

1488

8933

7590

06/15/2005

DUANE MORRIS, LLP

IP DEPARTMENT

ONE LIBERTY PLACE

PHILADELPHIA, PA 19103-7396

EXAMINER

DINH, SON T

ART UNIT

PAPER NUMBER

2824

DATE MAILED: 06/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

FE

Office Action Summary	Application No. 10/784,705	Applicant(s) CHEN ET AL.	
	Examiner Son T. Dinh	Art Unit 2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-27 is/are pending in the application.
4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-15 and 23-27 is/are allowed.
- 6) ☒ Claim(s) 16 and 18 is/are rejected.
- 7) ☒ Claim(s) 17 and 19-22 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>4/12/04</u> . | 6) <input checked="" type="checkbox"/> Other: <u>East search history</u> . |

DETAILED ACTION

Claim Rejections - 35 USC § 112

Claim 18 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The terminology "the threshold voltage" lacks a proper antecedent basis. It is not clear to what element (transistor, resistor) this threshold voltage refer to? Is it the threshold voltage of MOS transistor or what, if this is the case, then no transistor has been recited in claim 16, which this claim depends on. It is noted that every transistor have a threshold voltage (the minimum voltage to turn that transistor on).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 16 is rejected under 35 U.S.C. 102(e) as being anticipated by Rao et al (U.S., Patent No 6,208,549).

Figure 1 of Rao et al discloses a memory device comprising a first polycrystalline resistor (121, also see column 4, lines 2-3 which shows that the resistors are polycrystalline silicon) having a first end (the upper end of 121) connected to a first

Art Unit: 2824

control voltage level (VDD, through transistors 104 and 108), and a second end (the lower end of 121) connected to a second voltage level (ground), a second polycrystalline resistor (122) having a first end (the upper end of 122) connected to the first control voltage level (VDD, through transistors 103 and 107), and a second end (the lower end of 122) connected to the second voltage level (ground), wherein the first and second control voltage levels are imposed to program either the first or second (in this case, the first would be programmed, see column 4, lines 52-63) by causing a current stress (when transistor 102 is turn ON) across the resistor for programming the memory circuit.

No art rejection applied to claim 18 at this time, since the scope of the claim is not defined as stated above and no search could be performed.

Allowable Subject Matter

Claims 1-15, 23-27 are allowed.

Claims 17, 19-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record fail to teach or suggest a memory circuit comprising a data read module having first and second outputs, a first polycrystalline resistor having first end connected to a first control voltage, a second end connected to a second control

Art Unit: 2824

voltage level, a second polycrystalline resistor having first end connected to a first control voltage level, a connection module for connecting the first ends of the first and second transistors to the first and second inputs (claim 1); a method of programming by disabling the connection module, imposing the first control voltage and relieving the first control voltage using the circuit as claimed in claim 1 (claim 10); the selection of first control voltage level (3.3V) that is higher than the operating voltage (claim 17); the connection of a latch mode to the resistors (claim 19); a programming triggering module connected to the first and second resistors (claim 21); and wherein the resistance of the first resistor is lowered as compared to the unstressed second resistor (claim 23).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

-Mohsen et al disclose a memory device having a resistor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Son T. Dinh whose telephone number is 571-272-1868. The examiner can normally be reached on Monday to Friday 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2824

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

S. Dinh
June 11, 2005



Son T. Dinh
Primary Examiner